(12) UK Patent Application (19) GB (11) 2 157 489 A

(43) Application published 23 Oct 1985

(21) Application No 8507524

(22) Date of filing 22 Mar 1985

(30) Priority data

(31) 59/054286 (32) 23 Mar 1984 (33) JP
59/056029 26 Mar 1984

(71) Applicants
Hitachi Ltd (Japan)
6 Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, Japan
Hitachi Microcomputer Engineering Ltd (Japan)
1479 Josuihoncho, Kodaira-shi, Tokyo, Japan

(72) Inventors
Masahiro Ogata
Hiroshi Ishii
Shinji Shimizu

(74) Agent and/or Address for Service
Mewburn, Ellis & Co., 2/3 Cursitor Street, London EC4A 1BQ

(51) INT CL[4]
G11C 11/40 H01L 27/08

(52) Domestic classification
H1K 11A3 11C1A 11C1B 11D1 11D 1CA 1DE 4C11 4C14 4C1C 9C2 9D1 9N3 GAB
H3T 2B7 2T3F 2T3S MX
U1S 2121 H1K H3T

(56) Documents cited
None

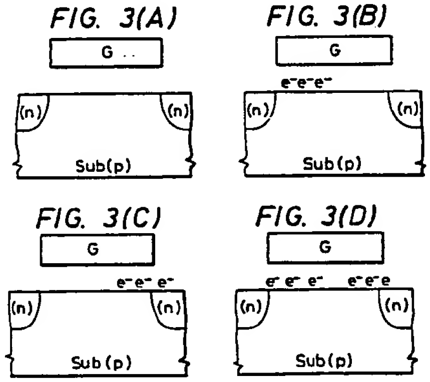
(58) Field of search
H1K

(54) A semiconductor integrated circuit memory device

(57) In a semiconductor memory device provided with a plurality of memory cells each comprised of an insulated gate field effect transistor having first and second semiconductor regions of a first conductivity type formed separately from one another in a substrate of a second conductivity type, two bits can be stored in each transistor.

The threshold voltages of the portions adjacent to the first region and/or the second region are raised by writing data. Since data can be written in at either the first or second regions, two bits can be effectively stored in each insulated gate field effect transistor. The first bit is read out under the state in which the first region serves as the drain and the second region, as the source, and the second bit is read out under the state in which the first region serves as the source and the second region, as the drain.

FIG. 3(A) FIG. 3(B) FIG. 3(C) FIG. 3(D)



GB 2 157 489 A

POOR QUALITY

2157432

1/12

FIG. 1

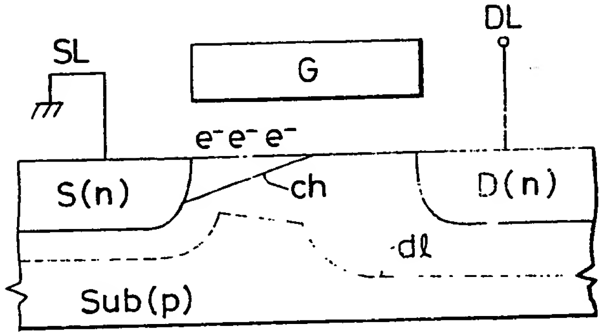


FIG. 2

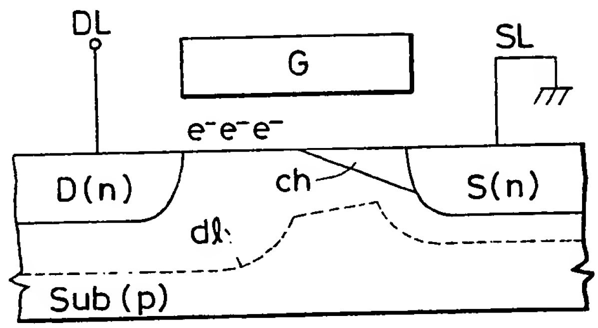


FIG. 3(A)

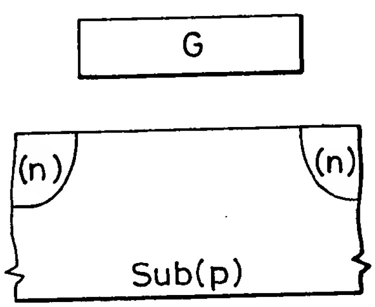


FIG. 3(B)

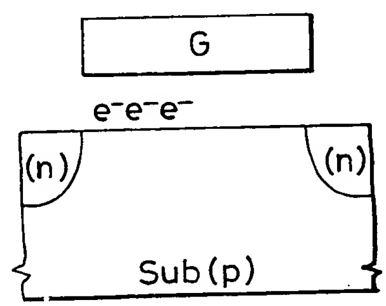


FIG. 3(C)

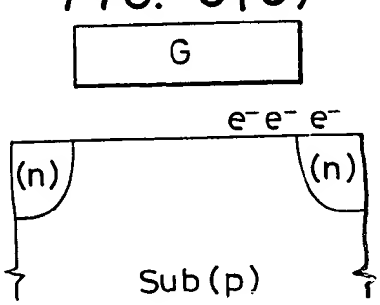
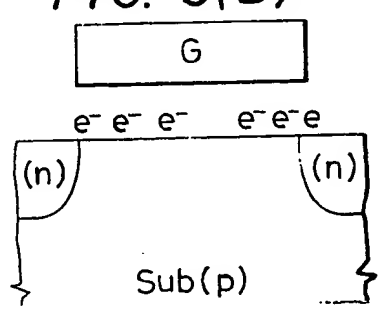


FIG. 3(D)



POOR QUALITY

2157489

2/12

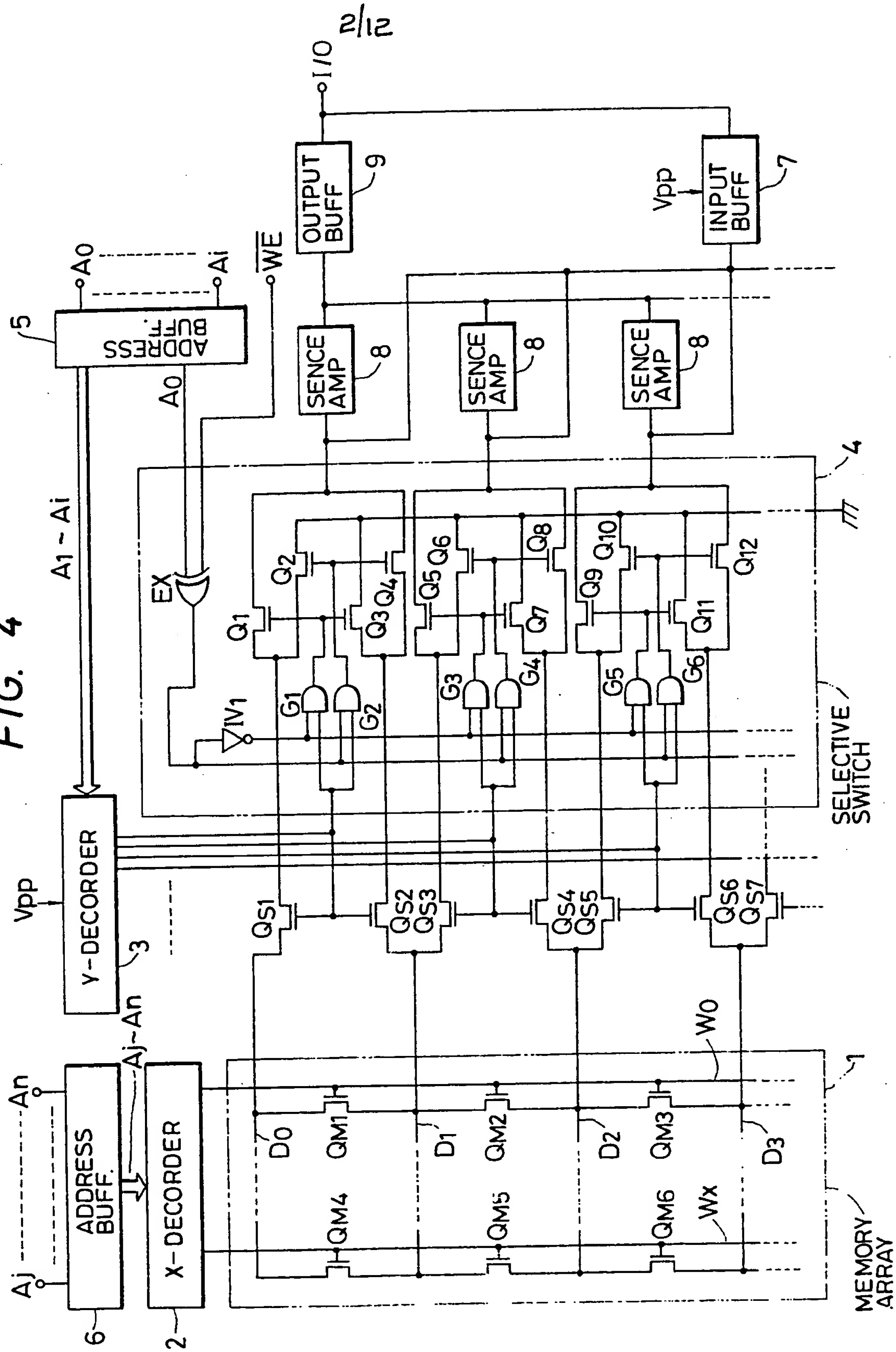


FIG. 4

FIG. 5

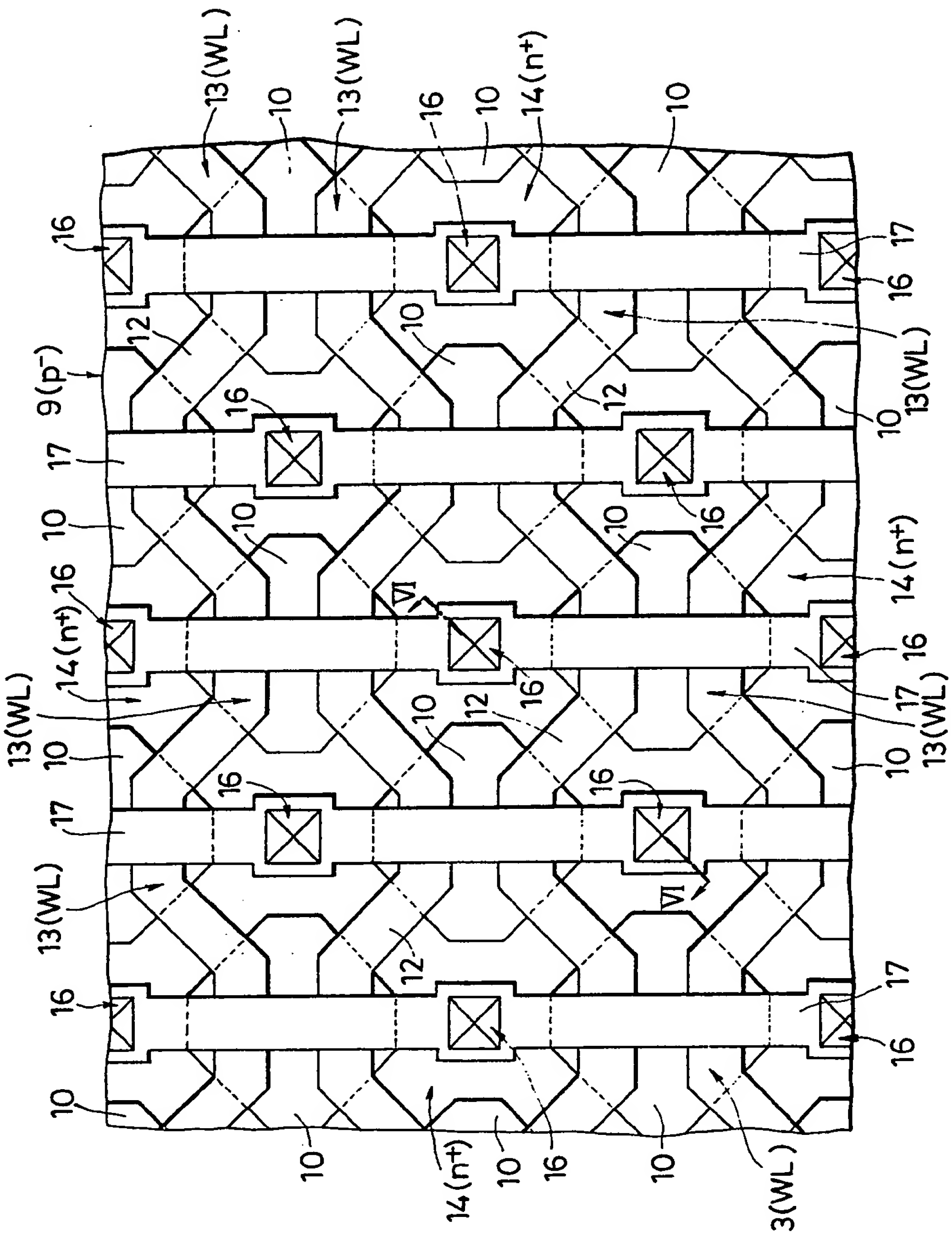


FIG. 6

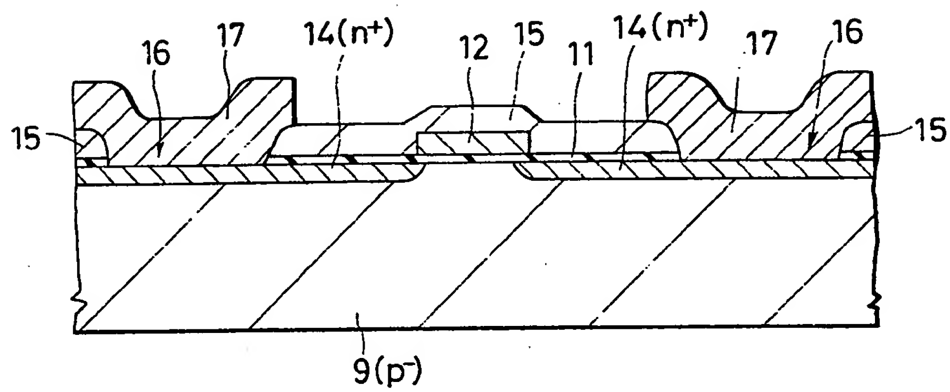

16
17
14(n+)
12
15
11
14(n+)
17
16
15
15
9(p-)

FIG. 8

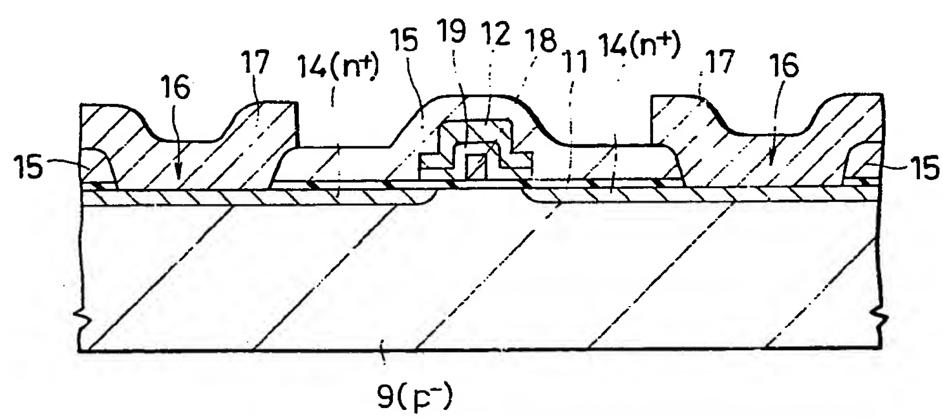

16
17
14(n+)
15
19
12
18
11
14(n+)
17
16
15
15
9(p-)

FIG. 7

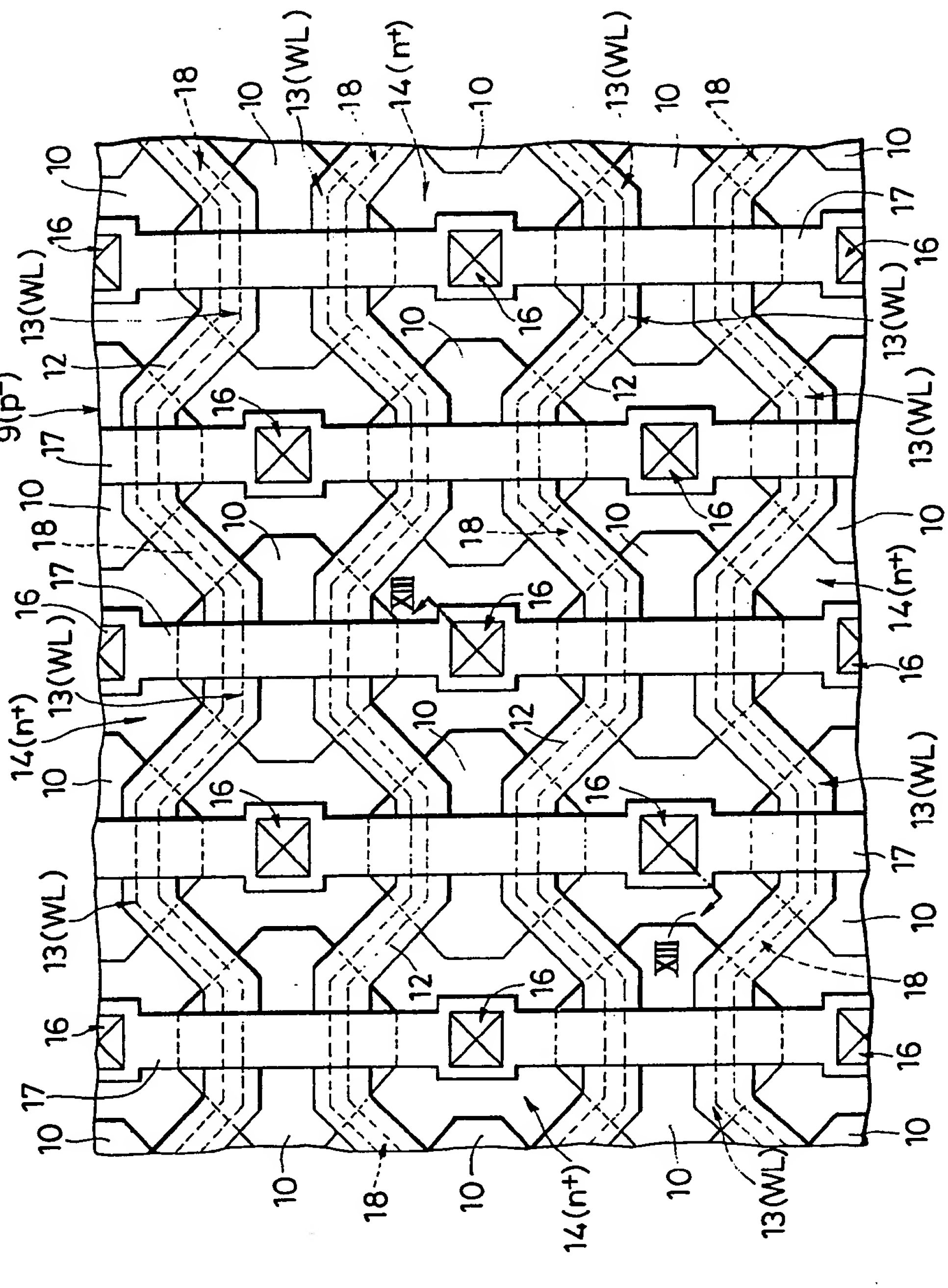


FIG. 9

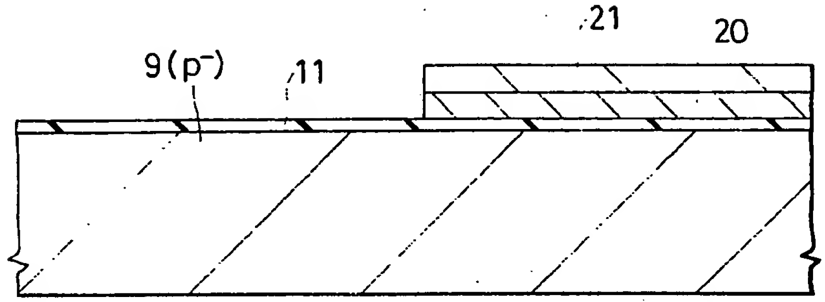


FIG. 10

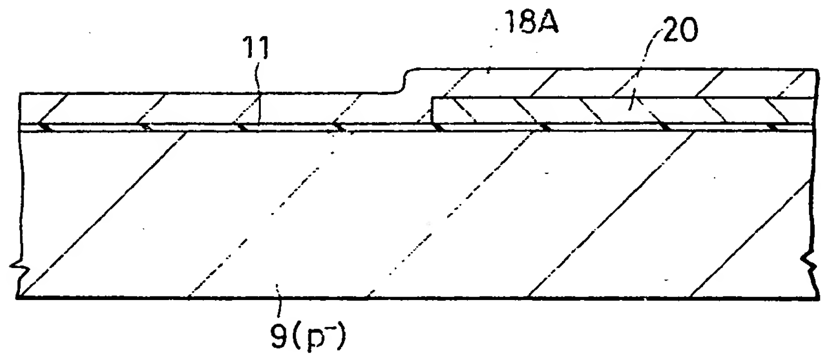


FIG. 11

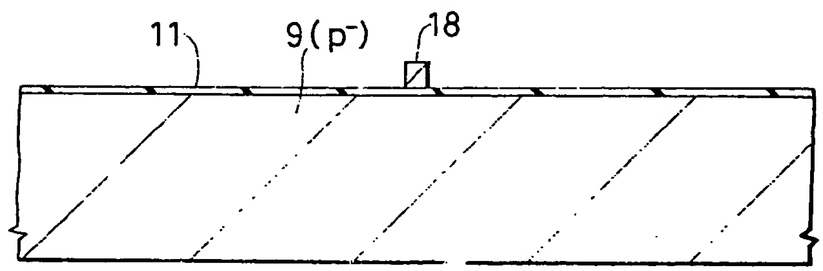


FIG. 12

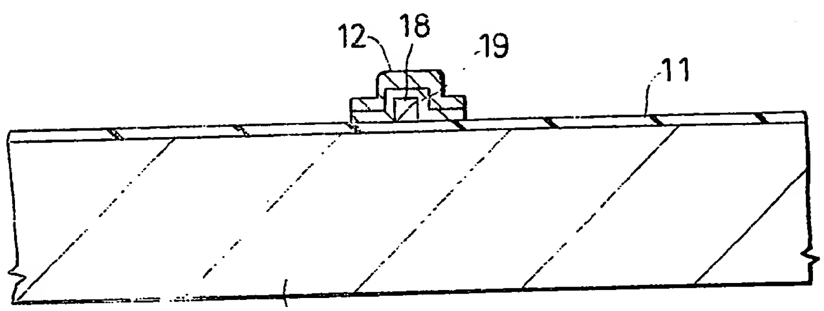
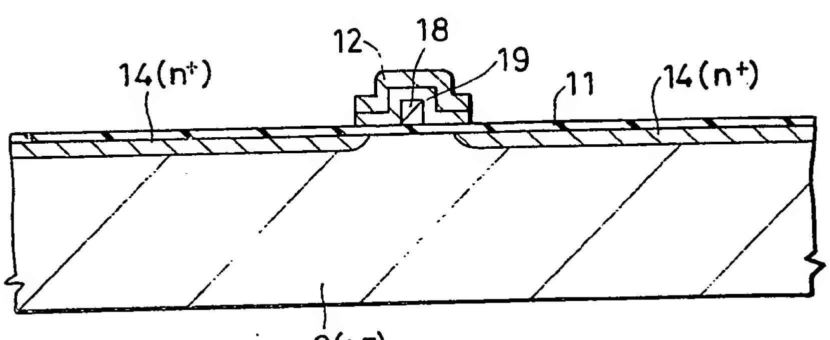


FIG. 13



2157439

8/12

FIG. 14

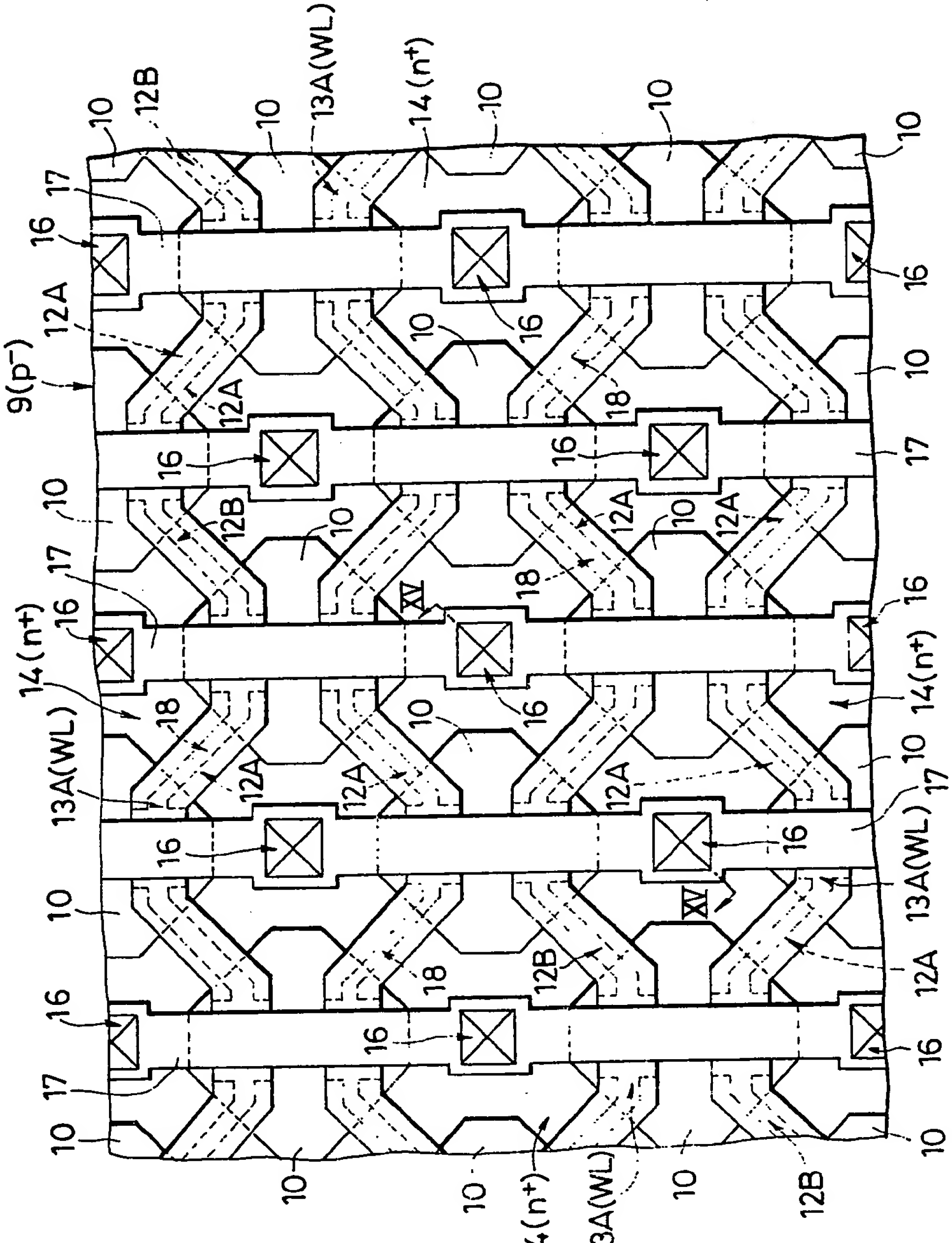


FIG. 15

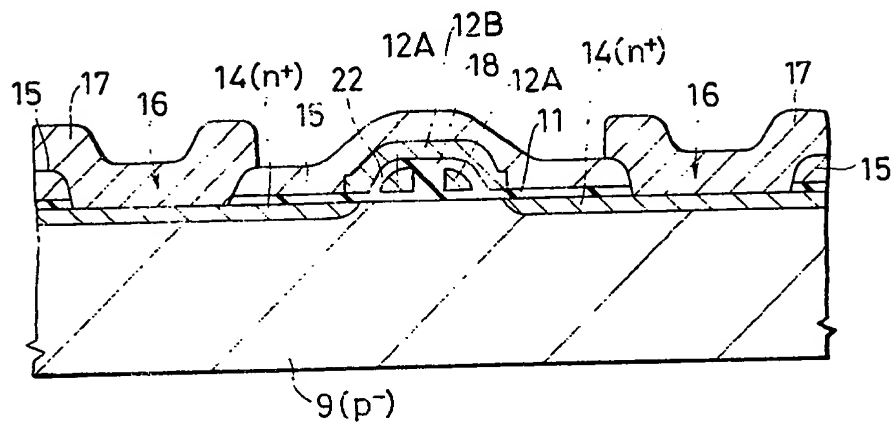


FIG. 16

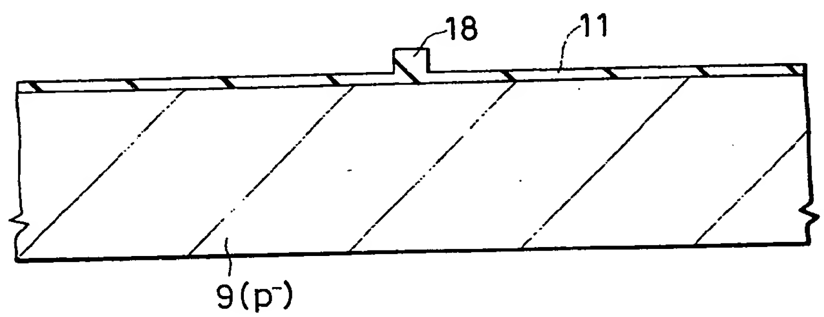


FIG. 17

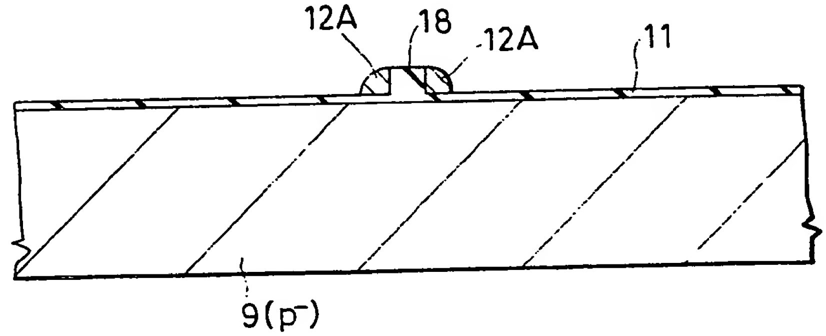


FIG. 18

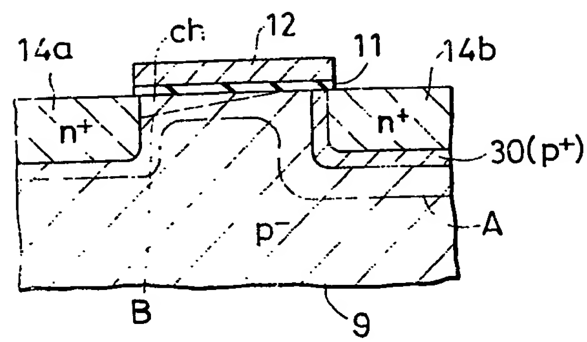


FIG. 19(A)

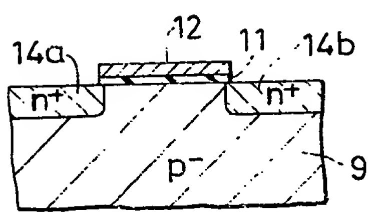


FIG. 19(B)

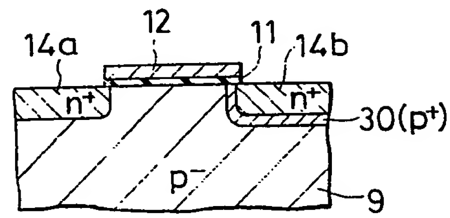


FIG. 19(C)

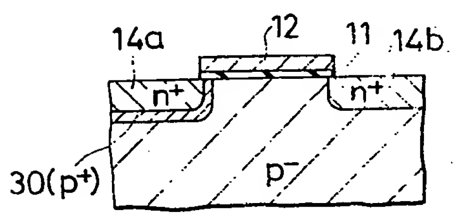


FIG. 19(D)

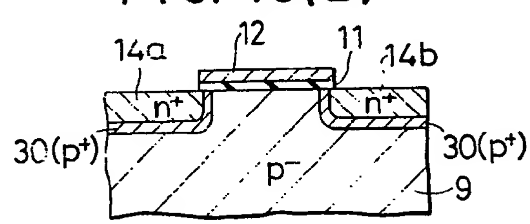


FIG. 21

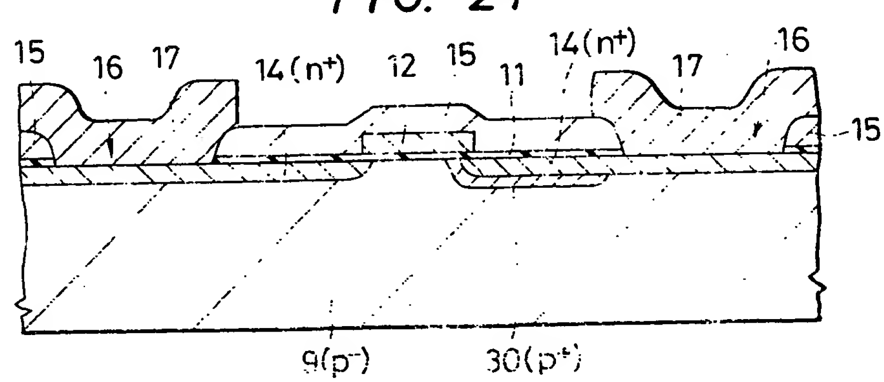
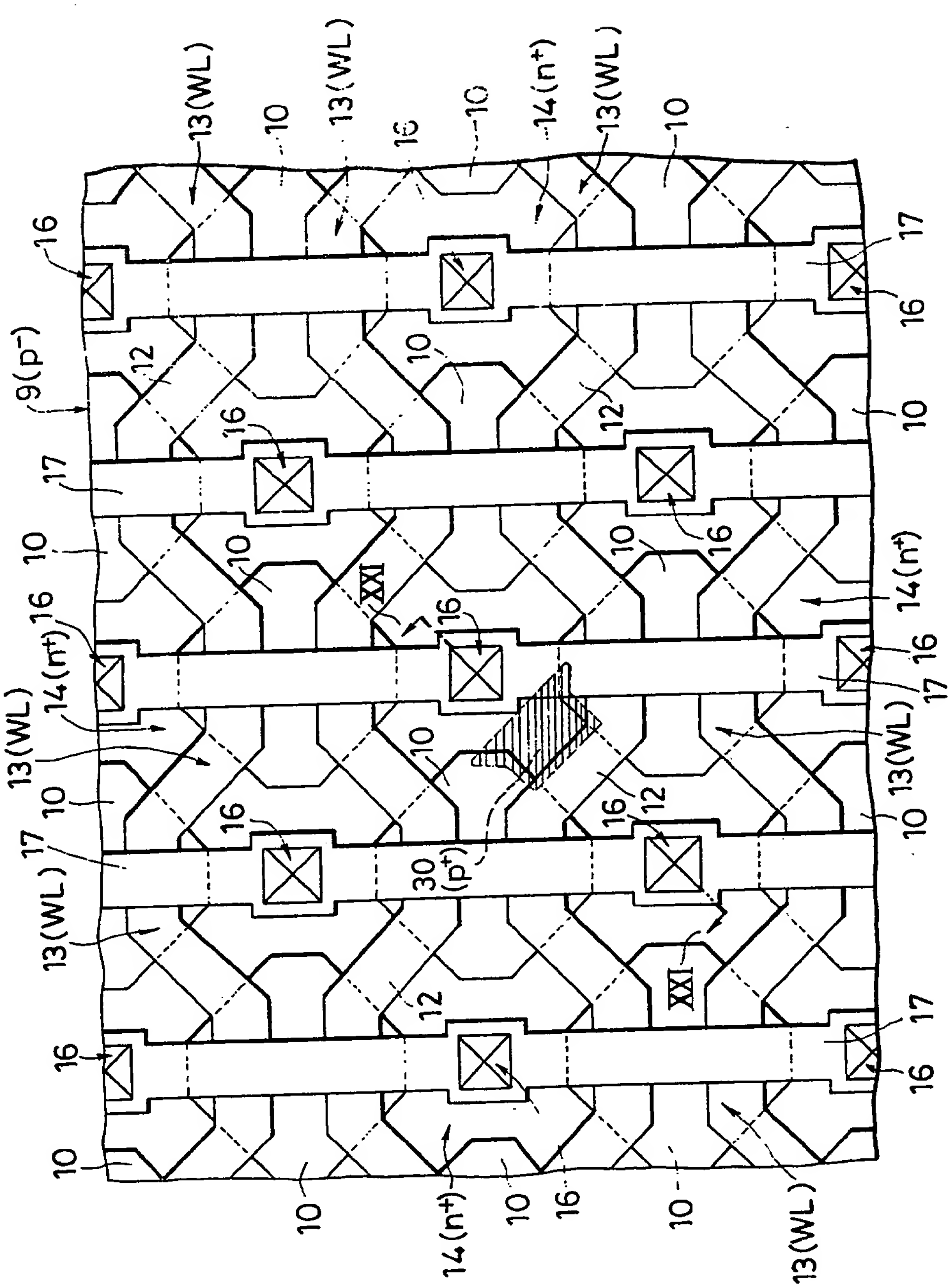
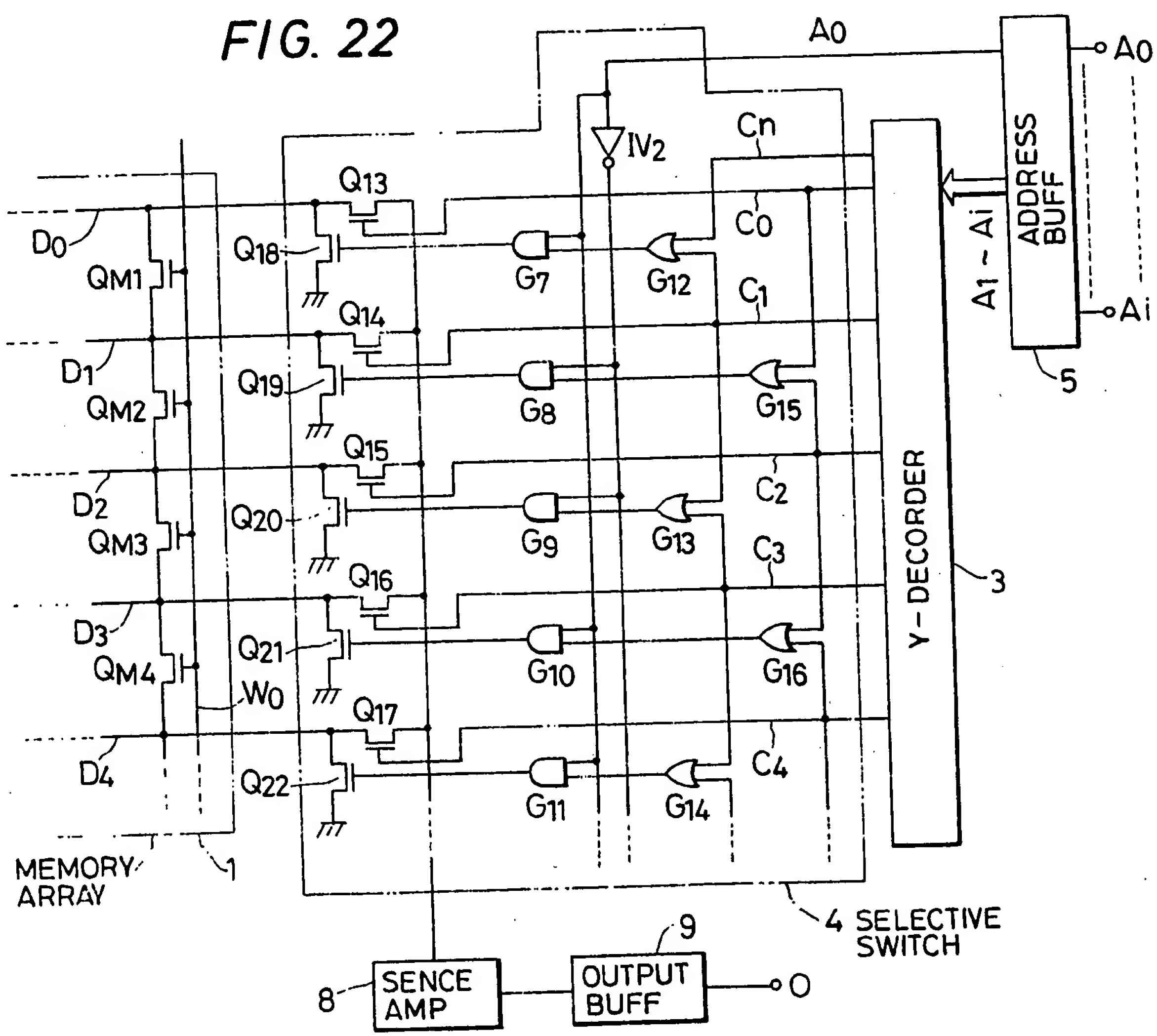


FIG. 20



12/12

FIG. 22



A0
A0
Ai
ADDRESS BUFF
5
A1 ~ Ai
Y-DECORDER
3
Cn
C0
C1
C2
C3
C4
IV2
G7
G8
G9
G10
G11
G12
G13
G14
G15
G16
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
D0
D1
D2
D3
D4
QM1
QM2
QM3
QM4
W0
MEMORY ARRAY
1
4 SELECTIVE SWITCH
8
SENCE AMP
9
OUTPUT BUFF
O

SPECIFICATION

A semiconductor integrated circuit device

The present invention relates to a technique which is effective when applied to a semiconductor integrated circuit device and, more particularly, to a technique which is especially effective when applied to a semiconductor integrated circuit having a read only memory fuction (which device will be shortly referred to as a "memory IC"), although not necessarily limited thereto.

In recent years, there has been a strong tendency for memory ICs such as ROMs (i.e., read only memory) or EPROMs (i.e., erasable and programmable ROM) to be highly integrated so as to increase the storage capacity thereof. In such memory ICs, the memory cells are generally each composed of an insulated gate type field effect transistor (which will be hereinafter referred to as a "MISFET") which can only store data of only 1 (bit). As a result, in order to increase the storage capacity up to about 1 (Mbit), for example, there is required an ultrafine lithography technique which has a minimum lithography size of less than 1 (μm) in the fabrication process. However, since such ultrafine lithography generally cannot be executed due to the limits of present day photolithography depending upon optical resolving power, and since the so-called short channel effect is induced when an effective channel length comes to about 2 (μm), we have found as a result of our investigations that there is presently a limit to the degree of integration possible with conventional MISFETs, and this makes it highly difficult to effect high integration of the memory IC.

It is an object of the present invention to provide an arrangement which is capable of highly increasing the capacity of a memory IC.

Another object of the present invention is to provide an arrangement capable of writing a plurality of bits of data into each memory cell composing a memory IC.

A further object of the present invention is to provide an arrangement which is capable of both writing a plurality of data bits into each memory cell composing a memory IC and holding the data stably within each such memory cell.

The above and other objects and novel features of the present invention will become apparent from the following description taken with reference to the accompanying drawings.

A representative example of the invention to be disclosed hereinafter will now be briefly described.

Specifically, depending upon whether threshold voltage of a MISFET for providing a memory cell is high or low at the side or sides of the source and/or drain regions of the MISFET, one memory cell can hold a plurality of data bits so that the capacity of the memory IC can be increased to a high value.

Y address signals are divided into a first group consisting of one or a plurality of address signals and a second group consisting of the rest, a plurality of data lines are selected by the second group for memory cell selection, and the condition of the data lines selected by the first group is determined. According to this arrangement, read-out and/or write-in of a plurality of data in and from one memory cell becomes possible.

Figs. 1 and 2 are schematic sectional views showing the essential portions of a MISFET constructing a memory cell for explaining the principle of the present invention;

Figs. 3(A) to 3(D) are schematic sectional views showing the essential portions of a MISFET constructing the memory cell under different write-in conditions for explaining the combination of the principles of the present invention to permit storage of two bits of information in one memory cell;

Fig. 4 is a schematic block diagram showing a system of the memory IC for operation in conjunction with memory cells such as shown in Figs. 1 to 3 for explaining the embodiment I of the present invention;

Fig. 5 is a top plan view showing the essential portion of the memory cell array for explaining the embodiment I of the present invention;

Fig. 6 is a sectional view taken along line VI-VI of Fig. 5;

Fig. 7 is a top plan view showing the essential portion of the memory cell array for explaining the embodiment II of the present invention;

Fig. 8 is a sectional view taken along line VIII-VIII of Fig. 7;

Figs. 9 to 13 are sectional views showing the essential portions of the memory cell array at the individual fabrication steps for explaining the fabrication process of the embodiment II of the present invention;

Fig. 14 is a top plan view showing the essential portion of the memory cell array for explaining the embodiment III of the present invention;

Fig. 15 is a sectional view taken along line XV-XV of Fig. 14;

Figs. 16 and 17 are sectional views showing the essential portions of the memory cell array at the individual fabrication steps for explaining the fabrication process of the embodiment III of the present invention;

Figs. 18 are schematic sectional views showing the essential portions of a MISFET constructing a memory cell for explaining the principle of the present invention;

Figs. 19(A) to 19(D) are schematic sectional views showing the essential portions of a MISFET constructing the memory cell under different write-in conditions for explaining the combination of the principles of the present invention to permit storage of two bits of information in one memory cell;

Fig. 20 is a top plan view showing the essential portion of the memory cell array for explaining the embodiment IV of the present invention;

Fig. 21 is a sectional view taken along line XXI-XXI of Fig. 20; and

Fig. 22 is a schematic block diagram showing a system of the memory IC for operation in conjunction with memory cells such as shown in Figs. 18 to 21 for explaining the embodiment IV of the present invention;

The present invention will be described in the following in connection with the embodiments thereof.

Embodiment I:

First of all, the principle of the present invention will

be explained.

Figs. 1 and 2 are schematic sectional views showing essential portions of a MISFET composing a memory cell for explaining the principle of the present invention.

In Figs. 1 and 2, reference letters Sub indicate a p-type semiconductor substrate; letter D indicates an n-type drain region; and letter S indicates an n-type source region. Reference letter G indicates a gate electrode which is formed over a semiconductor substrate through a gate insulating film (not shown). Letters DL indicate a data line which is connected with the drain region, and letters SL indicate a select line which is connected with the source region. Letters dl indicate a depletion layer which is formed to extend from the drain region D and the source region S into the semiconductor substrate Sub, and letters ch indicate a channel region which is formed at the side of the source region S by the gate electrode. Letters e^- indicate hot carriers which are injected during a write-in operation into the gate insulating film at the side of the drain region D or the source region S thereby to hold a plurality of data bits in the memory cell in a manner which will hereinafter be described.

Now, the gate electrode G is set at a potential of high level (which will be referred to as an "H level"), and the data line DL is set at the H level whereas the select line SL is set at a potential of low level (which will be referred to as an "L level"). Then, as shown in Fig. 1, there is established through a writing operation a state in which the hot carriers e^- exist in advance of the reading operation inside the gate insulating film at the side of the source region S. As a result, a threshold voltage (V_{th}) of a region to be formed with the channel region ch is raised to a higher value than that which existed before the hot carriers were injected. As a result, the MISFET is not rendered conductive, even if the gate electrode G is at the H level. Therefore the data line DL is held at the H level.

Next, as shown in Fig. 2, the data line DL and the select line SL are interchanged while the hot carriers e^- remain next to the left region (which now becomes the drain due to the data line DL). Then, the inside of the gate insulating film at the side of the source region is in the state having no hot carriers e^- existing, and the threshold voltage (V_{th}) of the region to be formed with the channel region ch is not increased from its original level before injection of the hot carriers e^-. As a result, the MISFET is in an ON state when the gate electrode G is at the H level so that the data line DL level drops from the H level substantially to the level of the select line SL, i.e., the L level.

In other words, it is assumed that the state of Fig. 1, in which the data line DL is at the H level, is a data bit of 1 whereas the state of Fig. 2, in which the data line DL is at the L level, is a data bit of 0. With this arrangement, two bits of data can be held by means of the single memory cell simply by considering one bit with the select and data lines in a first position and considering the other bit with the select and data lines interchanged.

On the basis of this principle, the write-in and read-out of the data in and from the memory cell are shown and tabulated in respect of their combination in Figs. 3(A) to 3(D) and in Table 1, respectively.

TABLE 1

Reading Method		Data			
Left	Right	(A)	(B)	(C)	(D)
S	D	0	1	0	1
D	S	0	0	1	1
Comb.	Data	0,0	1,0	0,1	1,1

As shown in Figs. 3(A) to 3(D) and tabulated in Table 1, in the MISFET shown in Fig. 3(A), the data line DL is held at the L level, no matter which of the n-type semiconductor regions at the right or left side might be made of the drain region D, so that the data 0 and 0 can be read out. In the MISFET shown In Fig. 3(B) (which corresponds to Figs. 1 and 2), the data line DL is held at the H level, if the right-hand side is made of the drain region D, and is changed from the H level to the L level, if the left-hand side is made of the drain region D, so that the data 1 and 0 can be read out. In the MISFET shown in Fig. 3(C), the data line DL is changed from the H level to the L level, if the right-hand side is made of the drain region D, and is held at the H level, if the left-hand side is made of the drain region D, so that the data 0 and 1 can be read out. In the MISFET shown in Fig. 3(D), the data line DL is held at the H level, no matter which of the right-hand side or the left-hand side regions might be made of the drain region D, so that the data 1 and 1 can be read out.

Next, an emboidment I of the present invention will be described in the following in connection with the specific construction thereof.

Fig. 4 is a schematic block diagram showing a system of the memory IC for explaining the embodiment I of the present invention.

In all the figures, incidentally, the units having the same functions are indicated at the same reference characters, and their repeated explanations are omitted.

In Fig. 4, reference numeral 1 indicates a memory array which is composed of a plurality of memory cells $Q_{M1} \sim Q_{M6}$ arrayed in the form of a matrix to hold data. Indicated at numeral 2 is an X-decoder for selecting a predetermined one of a plurality of word lines $W_o \sim W_x$, which extend in a row direction in the memory cell array 1. (In the following, the direction in which the word lines extend will be called the "row direction".) Numeral 3 indicates a Y-decoder for selecting a predetermined pair of a plurality of data lines $D_0 \sim D_3$ which extend in a column direction in the memory cell array 1. (In the following, the direction in which the data lines extend will be called the "Column direction".)

Each memory cell comprises of MISFET Q_M, and is disposed so as to correspond to a point of intersection between a word line and a data line. The gate electrode of MISFET Q_M is connected to a word line $W_o \sim W_x$, and its source or drain region, to a data line $D_0 \sim D_3 \ldots,$.

Symbols $Q_{S1} \sim Q_{S7}$ represent column switches each consisting of MISFET that receives the output of the Y decoder 3 at its gate electrode. Either one of the source and drain regions of MISFET Q_S is connected to the data line. In order to pair two adjacent data

lines, the same output of the Y decoder is applied to the gate electrodes of the column switches to be connected to the adjacent data lines. The data lines having two adjacent data lines are connected to two column switches.

Indicated at numeral 4 is a data line selective switching circuit for switching one of the paired data lines, which has been selected by the Y-decoder 3, into a select line.

The other of the source and drain regions of MISFET Q_S is connected tt the selective switch 4. The output of the Y decoder 3 is also applied to the selective switch 4, whose detail will be described elsewhere.

Numeral 5 indicates an address buffer circuit for assigning the address of the data line or the select line of the Y-decoder 3 and the data line selective switching circuit 4 in response to address signals A_0 to A_i. Whether the wiring connected with the memory cell is to be used as the data line or the select line may be determined by one of the address signals A_0 to A_i, e.g., the most significant digit A_0. Numeral 6 indicates an address buffer circuit for assigning the address of the word lines of the X-decoder 2 in response to address signals A_j to A_n. Numeral 8 indicates a sense amplifier for judging the minute data 1 and 0 of the selected memory cell to amplify the same. Indicated at numeral 9 is an output buffer circuit which is connected to a terminal I/O, and from which the output data is to be read. Numeral 7 indicates an input buffer circuit which is connected to the terminal I/O, and from which the input data is to be write.

The selective switch 4 comprises of a plurality of units disposed so as to correspond to two column switches connected to the same output terminal of the Y decoder, an exclusive OR gate EX and an inverter IV_1 for inverting the output of the gate EX. The unit comprises of AND gates G_1 and G_2, and N-channel MOSFETs $Q_1 \sim Q_4$. The output of the inverter IV_1 is applied to one of the input terminals of the gate G_1, and the output of the gate EX is applied to one of the input terminals of the gate G_2. The output of the Y decoder is applied to the other terminal each of the gates G_1 and G_2.

On the other hand, MOSFETs Q_1 and Q_2 are connected in series with the column switch Q_{s1}, and MOSFETs Q_3 and Q_4 are connected in series with the column switch Q_{s2}. The output of the gate G_1 is applied to the gate electrodes of MOSFETs Q_1 and Q_3, and the output of the gate G_2, to the gate electrodes of MOSFETs Q_2 and Q_4. One of the source and drain regions of each of MOSFETs Q_1 and Q_4 is connected to a common sense amplifier 8 or to an input buffer 7. One of the source and drain regions of each of MOSFETs Q_2 and Q_3 is connected to the ground potential of the circuit. The units consisting of the AND gates $G_3 \sim G_6$ and N-channel MOSFETs $Q_5 \sim Q_{12}$ are disposed in such a manner as to correspond to the two column switches connected to the same output terminal of the Y decoder, that is, to the paired data line, in the same way as the unit consisting of the gates G_1 and G_2 and MOSFETs $Q_1 \sim Q_4$ described above. The AND gates $G_1 \sim G_6$ can be constituted, for example, by conventional NAND gates consisting of four N-channel MOSFETs and an inverter consisting of two N-channel MOSFETs and receiving the output of the NAND gates as its input. The afore-mentioned address signal A_0 is applied from the address buffer circuit 5 to one of the input terminals of the exclusive OR gate EX, and a write enable signal (write control signal) $\overline{WE}$ is applied to the other input terminal. Upon receiving the write enable signal $\overline{WE}$, the gate EX produces the inverted signal of the address signal A_0 at the time of read-out, and produces as such the address signal A_0 at the time of write-in. The role of the gate EX will be described elsewhere.

On the other hand, the data bits of the memory cell selected are written in and read out again by interchanging the selected data and select lines after the write-in and read-out of the same have once been executed with the originally selected data and select lines to allow for obtaining 2 bits of data from each memory cell, as previously discussed.

Next, the memory cell array will be described in the following in connection with the specific construction thereof.

Fig. 5 is a top plan view showing an essential portion of the memory cell array for explaining the embodiment I of the present invention, and Fig. 6 is a sectional view taken along line VI-VI of Fig. 5. In Fig. 5, incidentally, the insulating films formed between the individual conductive layers are omitted so that the figure may be seen clearly.

In Figs. 5 and 6, reference numeral 9 indicates a p^--type semiconductor substrate which is made of a single crystal silicon for constructing the memory IC. Indicated at numeral 10 is a field insulating film over the main surface of the semiconductor substrate 9 between regions, which are to be formed with the semiconductor element, so as to isolate the same electrically. Indicated at numeral 11 is an insulating film which is formed on the main surface of the semiconductor substrate 9 in the regions, which are to be formed with the semiconductor element, thereby to construct mainly the gate insulating film of the MISFET. The hot carriers can be injected into the insulating film 11 at the side or sides of the source region S and/or the drain region D of the MISFET. Numeral 12 indicates a conductive layer which is formed on a predetermined portion of the insulating film 11 thereby to construct the gate electrode of the MISFET. Indicated at numeral 13 is a conducting layer which is connected electrically with the conducting layer 12 located in the vicinity thereto in the row direction and which is formed over the field insulating film 10 thereby to construct word lines WL. Indicated at numeral 14 are n^+-type semiconductor regions which are formed in the main surface of the semiconductor substrate 9 across the insulating film 11 at both sides of the conductive layer 12 and which are used as the source region S or the drain region D thereby to construct the MISFET. Thus, the MISFET constructing the memory cell is composed mainly of the semiconductor substrate 9, the insulating film 11, the conducting layer 12 and the paired semiconductor regions 14. Indicated at numeral 15 are insulating films which are formed to cover the semiconductor element thereby to effect electrical isolation from conducting layers to be formed thereabove. Indicated at numeral 16 are connecting holes which are formed

by selectively removing the insulating films 11 and 15 over predetermined portions of the semiconductor regions 14. Indicated at numeral 17 are conductive layers which are connected electrically with the semiconductor regions 14 through the connecting holes 16 and which are formed to extend in the column direction over the insulating films 15 and which are used as the data lines DL or the select lines SL.

Next, the specific operations of the present embodiments will be described briefly with reference to Figs. 4 to 6.

First of all, the operation for writing data 1 and 1 into the memory cell of the MISFET will be described.

During the operation for writing, the input impedance and output impedance of the output buffer circuit 9 and the sense amplifier 8 are raised extremely high by the write enable signal $\overline{WE}$, for example. As a result, these circuits 8 and 9 are cut off from the other circuit portions. The data that is applied to the input/output terminal I/O and is to be written into the memory cell is applied to the input beffer circuit 7.

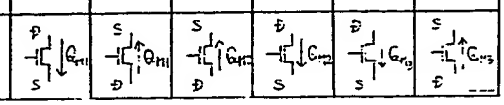
During the operation for writing, a write-in voltage V_{pp} (e.g., about 12 volts, although a voltage as high as 17 to 20 volts could be used) is supplied to the input buffer circuit. The input buffer circuit 7 produces the write-in voltage V_{pp} when the data is at the H level (typically the power supply voltage V_{cc} level of 5 volts), and produces as such the L level when the data is at the L level (typically about the ground potential V_{ss} level of 0 volts). The output voltage of the input buffer circuit 7 is supplied to the selective switch 4.

The write enable signal $\overline{WE}$ is at the L level during the operation for writing. When the L level signal $\overline{WE}$ is applied to one of the input terminals of the gate EX, the gate EX produces as such the address signal A_0 that is applied thereto during the operation for writing.

The (X) address signals A_j to A_n are applied to the address buffer circuit 6, and the H level (e.g./ aztut 5 (V)) is applied to the word line WL_0 (i.e., the conducting layer 13), which is selected by the x-decoder 2, so that the MISFET connected with said word line WL_0 is turned on.

While one data line such as WL_0, for example, is kept fixed at the H level, the function and potentials of the data lines D_0 through D_3 are sequentially set as tabulated in Table 2 below.

TABLE 2

cycle	1	2	3	4	5 (1)	6 (2)
D_0	DL	SL				
D_1	SL	DL	SL	DL		
D_2			DL	SL	DL	SL
D_3					SL	DL
current direction						

Among the Y address signals A_0 through A_i applied to the address buffer circuit, one address signal, e.g., the most significant digit A_0, is applied to the selective switch 4 while the rest A_1 through A_i are applied to the Y decoder 3.

In order to select one paired data line, e.g., D_0 and D_1, the Y decoder 3 applies the H level signal to the gate electrodes of MOSFETs Q_{s1} and Q_{s2} and the L level signals to the other MOSFETs Q_{s3} through Q_{s7} on the basis of the address signals A_1 through A_i. As a result, MOSFETs Q_{s1} and Q_{s2} become conductive, thereby connecting the data lines D_0 and D_1 to the selective switch 4. On the other hand, MOSFETs Q_{s3} through Q_{s7} become non-conductive, and the other data lines D_2 and D_3 are cut off from the selective switch 4. Let's consider the selective switch 4. Due to the output of the Y decoder 3 described above, the H level is applied to one of the input terminals of each of the gates G_1 and G_2, and the L level is applied to one of the input terminals of each of the gates G_3 through G_6. As a result, the gates G_3 through G_6 produced the L level even though either of the H and L levels is applied to the other input terminals. In consequence, MOSFETs Q_5 through Q_{12} become non-conductive.

On the other hand, the L level address signal A_0 and the H level inverted address signal $\overline{A_0}$ inverted by the inverter IV_1 are applied to the other input terminals of the gates GQ!E¼¼AND G_1. As a result, the gates G_1 and G_2 produce the H and L levels, respectively. Therefore, MOSFETs Q_1 and Q_3 become conductive, while MOSFETs Q_2 and Q_4 become non-conductive.

The data line D_0 is connected to the input buffer circuit 7 through MOSFETs Q_{s1} and Q_1 due to the operations of the Y decoder 3 and selective switch 4 described above, and the data line D_1 is connected to the ground potential of the circuit through MOSFETs Q_{s2} and Q_3. As a result, MISFET Q_{M1} as one memory cell is selected. Then, the data line D_0 becomes a data line DL connected to the drain region D of MOSFET Q_{M1} (i.e., the semiconductor region 14; this also holds true of Table 2 and so on). The data line D_1 becomes a data line SL connected to the source region S of MISFET Q_{M1} (i.e, semiconductor region 14; this also holds true of Table 2 and so on).

The write-in voltage V_{pp} is delivered from the input buffer circuit 7 to the data line DL (D_0) in response to the write-in data (H level). As a result, the hot carriers e^- are injected into the insulating film 11 at the side of

the drain region D, and the data 1 is thus written into the memory cell Q_{M1}.

In the manner described above, the first cycle of the operation for writing shown in Table 2 is completed.

Incidentally, when the data 0 is written, the L level is delivered from the input buffer circuit 7 to the data line DL (D_0) in response to the write-in data 0 (L level). Therefore, the data 0 is written because the hot carriers e^- are not injected into the insulating film 11.

Next, other one-bit data for the same memory cell (Q_{M1}) is written. This means that the second cycle shown in Table 2 is carried out.

First of all, a new Y address signal is taken into the address buffer circuit 5. In practice, since the same memory cell Q_{M1} is selected, the Y address signals A_1 through A_i are the same as those in the cycle 1. Since the functions of the data lines D_0 and D_1 are interchanged, the address signal A_0 changes from the L level to the H level. Therefore, the data line D_0 is connected to the ground potential of the circuit through MOSFETs Q_{s1} and Q_2 and becomes the data line SL. The data line D_1 is connected to the input buffer circuit 7 through MOSFETs Q_{s2} and Q_4 and becomes the data line DL. The write-in voltage V_{pp} is delivered from the input buffer circuit 7 to the data line DL (D_1) in response to the write-in data 1 (H level), and hence the other data 1 is written into the memory cell Q_{M1}.

In the manner described above, the write-in operation of the data bits 1 and 1 to one memory cell is completed.

In the practical operation for writing, it is better to scan the Y address while one word line such as WL_0, for example, kept fixed at the H level. In other words, it is better to sequentially carry out the procedures of the third cycle and so forth shown in Table 2. While the column switches Q_{s3} and Q_{s4} are selected by the Y decoder 3, the address signal A_0 is set to the H level to carry out the third cycle, and the address signal A_0 is then set to the L level to carry out the fourth cycle. As shown in Table 2, the fifth and sixth cycles have the same patterns as those of the first and second cycles, and the seventh and eighth cycles have the same patterns as the third and fourth cycles, though they are not shown in Table 2. In other words, the same pattern appears in every four cycles. After scanning of all the Y addresses is completed for the word line WL_0, the procedures are repeated sequentially up to the word line WL_x.

Next, the operations of reading out the data 1 and 1 of the MISFET for providing the memory cell will be described in the following.

During the operation of reading, the input and output impedance of the input buffer circuit 7 are raised by the write enable signal $\overline{WE}$, for example, and are cut off from the other circuits. During this period, the signal $\overline{WE}$ is at the H level, and hence the gate EX produces an inverted signal $\overline{A_0}$ obtained by inverting the input signal A_0 applied thereto.

Now, the case in which the data bits 1 and 1 written into the memory cell Q_{M1} is read out will be described.

In order to read out the data written during the cycle 1 of Table 2, the same address signals A_0 through A_n as those in the cycle 1 are applied. In the same way as in the cycle 1, the word line WL_0 is selected (is raised to the H level) by the X decoder 2, and the paired data lines D_0 and D_1 are selected by the Y decoder 3. (The H level is applied to the gate electrodes of the column switches Q_{s1} and Q_{s2}.) The L level address signal A_0 which is the same as when the cycle 1 is carried out is turned into the inverted signal $\overline{_0}$, that is, H level and is produced from the gate EX. The output of the gate G_1 falls to the L level and the output of the gate G_2 rises to the H level. Therefore, the data line D_0 is connected to the ground potential of the circuit through MOSFETs Q_{s1} and Q_{s2}. The data line D_1 is connected to the sense amplifier 8 and to the output buffer circuit 9 through MOSFETs Q_{s1} and Q_4. In other words, the relation between the data lines D_0 and D_1 is opposite to the relation when the data is written in the cycle 1.

Here, it is to be noted that the data written in the cycle 1 can not be read out if the relation betweeen the data lines D_0 and D_1 is the same as the relation in the cycle 1. It will be assumed, for example, that the cycle 1 is carried out under the state shown in Fig. 2 and the hot carrier e^- is injected to the left semiconductor region of Fig. 2. In this writing operation, the left semiconductor region is the drain region D (to be connected to the data line D_0) and the right semiconductor region is the source region S (to be connected to the data line D_1). Next, when the read-out operation is carried out under the same condition, the written hot carrier e^- does not exist on the channel region (inverted layer) CH (the state shown in Fig. 2). Therefore, the threshold voltage of the region, in which the channel region is to be formed, does not rise. As a result, the overall threshold voltage (V_{th}) of MISFET Q_{M1} hardly rises. If the H level is applied to the word line WL_0 under this state, MISFET Q_{M1} becomes conductive, and the potential of the data line D_0 drops to the potential of the data line D_1, that is, the ground potential of the circuit. Since this corresponds to the state of the data bit 0, the data 0 is written although the data 1 is written into the address described above.

In contrast, if the data, which is written by carrying out the write-in cycle 1 under the state shown in Fig. 2, is read out under the state shown in Fig. 1, the data 1 is read out. That is, in Fig. 1, the left semiconductor region connected to the data line D_0 is the source region S, and the right semiconductor region connected to the data line D_1 is the drain region. Under this state, since the written hot carrier e^- exists on the channel region CH, the threshold voltage at this portion becomes high, so that MISFET Q_{M1} does not become conductive even if the word line WL_0 is raised to the H level, and the data line D_1 holds the original level (H level).

The data bit written using the data line D_0 as DL and the data line D_1 as SL must be read out while changing the data line D_0 to SL and the data line D_1 to DL. Since read-out and write-in must be made by the same address signal, the gate EX is provided.

For the reason described above, the data 1 written into the memory cell Q_{M1} in the cycle 1 is read out by setting the word line WL_0 to the H level, the data line D_0 to SL and the data line D_1 to DL. The data line D_1 is pre-charged to the H level, or the H level is supplied thereto from the sense amplifier 8. Since the data written in the cycle 1 is 1, MISFET Q_{M1} is not conductive and the data line D_1 keeps the H level.

Incidentally, if the written data is 0, MISFET Q_{M1} becomes conductive, and the potential of the data line D_1 drops to the L level. The potential of the data line D_1 (DL) is sensed by the sense amplifier 8, and is delivered to the output buffer circuit 9.

Next, the address signal after the cycle 2 is carried out is taken, and the other data bit 1 written into MISFET Q_{M1} is read out in the same way as described above.

It should be noted at this point that the present invention can operate as an EPROM or an EEPROM (electrically erasable and programmable ROM). To this end, information written into the insulating film in the manner described previoiusly can be erased by such techneques as using ultraviolet rays or electric signals. When either of these methods is used, it is convenient to erase all the bits altogether. The ultraviolet rays may be radiated to the chip as a whole in the same wayyy as EPROM. When the electrical erasing method is employed, the semiconductor substrate 9 is kept at the V_{pp} potential, for example, and all the word lines are kept at the ground potential of the circuit.

As has been described hereinbefore, according to the present invention, the data of 2 (bits) can be held in the signal MISFET by injecting the hot carriers into the gate insulating film at the side or sides of the source region and/or the drain region of the MISFET constructing the memory cell of the memory IC and by writing the data by mutually inerchanging the data lines and the select lines. Since the data of 2 (bits) can be held by the single MISFET, moreover, the capacity of the memory IC can be increased to a remarkable value.

Embodiment II:

Next, an embodiment II of the present invention will be described in the following in connection with the specific construction thereof.

The present embodiment and a later-described embodiment III are presented for holding stably the hot carriers which are injected into the gate insulating film at the side or sides of the source region and/or the drain region of the MISFET.

Fig. 7 is a top plan view showing an essential portion of a memory cell array for explaining the embodiment II of the present invention, and Fig. 8 is a sectional view taken along line VIII-VIII of Fig. 7. In Fig. 7, incidentally, the insulating films to be formed between the individual conducting layers are omitted so that the same figure may be seen clearly.

In Figs. 7 and 8, reference numeral 18 indicates an insulating film which is formed over the insulating film 11 at the central portion between the semiconductor region 14 (i.e., between the source region S and the drain region D) thereby to hold the hot carriers e^- to be injected stably in the gate insulating film at the side or sides of the source region and/or the drain region D of the MISFET. More specifically, the thickness of the central portion of the insulating film 11 between the semiconductor regions 14 is substantially increased by the insulating film 18 to prevent the occurrence of a soft error which can be induced as a result of the hot carriers e^- injected into the source region S being caused to migrate to the drain region D by external circumstances, for example. Indicated at numeral 19 is an insulating film which is formed over both the insulating film 11 for providing the gate insulating film 18 thereby to provide the gate insulating film. The gate insulating film of the MISFET is composed of the insulating films 11, 18 and 19, and the hot carriers e^- are held in the intervening portion between the insulating film 11 and the insulating film 19.

Next, the specific process for fabricating the present embodiment will be described in the following.

Figs. 9 to 13 are sectional views showing the essential portion of the memory cell array at individual fabrication steps for explaining the fabrication method of the embodiment II of the present invention.

First of all, the p^--type semiconductor substrate 9 is prepared. After the field insulating film 10 has been formed, moreover, the insulating film 11 is formed. This insulating film 11 may be made of a silicon oxide film prepared by thermal oxidation, for example, to have a thickness of about 150 to 250 (Å). Next, in order to form the insulating film 18, a polycrystalline silicone film 20 is formed and is patterend by using a photoresist film 21 as an etching-resisting mask such that its end portion is positioned at the middle portion between the source region S and the drain region D, as shown in Fig. 9.

After the step shown in Fig. 9, an insulating film 18A is formed all over the surface, as shown in Fig. 10. The insulating film 18A may be made of a silicon oxide film prepared at a high temperature and under a low pressure, for example, to have a thickness of about 0.3 to 0.6 (μm).

After the step shown in Fig. 10, the whole surface is etched anisotropically to form the insulating film 18 in self-alignment at the end portion of the polycrystalline silicon film 20. As shown in Fig. 11, moreover, all of the polycrystalline silicon film 20 is removed at this time. The insulating film 18 may be formed to have a thickness of about 0.3 to 0.6 (μm) and a width of about 0.1 to 0.2 (μm).

After the step shown in Fig. 11, the whole surface is covered with such an insulating film as can provide the gate insulating film. The insulating film may be made of a silicon nitride film prepared by chemical vapor deposition (which will be abbreviated as "CVD"), for example, to have a thickness of about 1,000 to 2,000 (Å). Moreover, the whole surface is covered with such a conductive layer as can provide the word lines WL and the gate electrode.

The conductive layer may be made of a polycrystalline silicon film prepared by the CVD, for example, to have a thickness of about 2,000 to 3,000 (Å). After that, as shown in Fig. 12, the insulating films and the conductive layers are patterned selectively to form the insulating film 19, the conductive layer 12 and the conductive layer 13, which is not shown. Incidentally, the conductive layers 12 and 13 should not be limited to the polycrystalline silicon film but may be either made of a metal layer having a high melting point such as molybdenum or tungsten or a layer of a silicide, i.e., the compound of the high-melting point metal and silicon, or constructed to a two-layered construction of the polycrystalline silicon film and the

silicide layer of the metal of high melting point.

After the step shown in Fig. 12, the n^+-type semiconductor regions 14 are formed in the main surface of the semiconductor substrate 9 across the insulating film 11, as shown in Fig. 13, by using the conductive layer 12 as a mask for introducing the resisting impurity. The semiconductor regions 14 may be formed by ion implantation, for example.

After the step shown in Fig. 13, the insulating film 15, the connecting holes 16 and the conductive layer 17 are formed, as shown in Fig. 8. The insulating film 15 may be made of a phosphosilicate glass film, for example, and the conductive layer 17 may be made of an aluminum film, for example. The memory IC of the present embodiment is completed by the series fabrication steps thus far described.

After that, incidentally, the memory IC may be covered with a protective film.

Moreover, a conducting layer made of aluminum, for example, may be formed over the conducting layer 17 across the insulating film and connected electrically with the conductive layer 13 to extend in the same direction thereby to reduce the resistance of the conductive layer 13.

As has been described hereinbefore, according to the present embodiment, effects similar to those of the foregoing embodiment I can be attained.

Thanks to the provision of the thick insulating film 18 at the middle portion between the source region and the drain region of embodiment II, moreover, the hot carriers injected can be held more stably in the gate insulating film at the side or sides of the source drain region and/or the drain region of the MISFET.

Embodiment III:

Next, an embodiment III of the present invention will be described in the following in connection with the specific construction thereof.

Fig. 14 is a top plan view showing an essential portion of a memory cell array for explaining the embodiment III of the present invention, and Fig. 15 is a sectional view taken along line XV-XV of Fig. 14. In Fig. 14, incidentally, the insulating films to be formed between the individual conductive layers are omitted so that the same figure may be seen clearly.

In Figs. 14 and 15, reference character 12A indicates conductive layers which are formed in self-alignment over the insulating film 11 at both the sides of and relative to the insulating film 18 thereby provide floating gate electrodes for the MISFET. Indicated at numeral 22 is an insulating film which is an insulating film which is formed to cover the conductive layer 12A thereby to provide an inter-layer insulating film between the floating gate electrodes and control gate electrodes. Indicated at characters 12B is a conductive layer which is formed to cover the insulating film 22 thereby to provide the control gate electrode of the MISFET. Indicated at characters 13A is a conducting layer which is connected electrically with the conductive layer 12B in the vicinity thereof in the row direction and formed over the field insulating film 10 thereby to provide the word lines WL.

Next, the specific fabrication process of the present embodiment will be described in the following.

Figs. 16 and 17 are sectional views showing essential portions of the memory cell array at the individual fabrication steps for explaining the fabrication process of the embodiment III of the present invention.

First of all, after the field insulating film 10 has been formed over the main surface of the semiconductor substrate 9, an insulating film having a thickness of about 0.3 to 0.6 (µm) is formed. By the photolithography and the anisotropic etching, moreover, the insulating film is patterned to form the insulating film 18 at the middle portion between the source region S and the drain region D. After that, as shown in Fig. 16, the insulating film 11 is formed over the main surface of the semiconductor substrate 9 other than the insulating film 18 by the thermal oxidation.

After the step shown in Fig. 16, the conductive layers 12A are formed, as shown in Fig. 17. The conductive layers 12A may be made of a polycrystalline silicon film, for example, by the technique which is similar to that used at the step of forming the insulating film 18 in the foregoing embodiment II.

After the step shown in Fig. 17, the insulating films 12A are formed by the thermal oxidation, and the conductive layer 12B and the conductive layer 13A are formed thereover. By the step sihilar to that of the foregoing embodiment II, moreover, the memory IC of the present embodiment is completed, as shown in Fig. 15.

As has been described hereinbefore, according to the present embodiment III, effects similar to those of the foregoing embodiments I and II can be attained.

Embodiment IV:

The present invention can be applied not only to an erasable ROM but also to a non-erasable ROM, that is, a mask ROM. The principle when the present invention is applied to the mask ROM will be described with reference to Fig. 18.

Fig. 18 shows the structure of an N-channel MOSFET. N^+-type regions 14a and 14b that are to serve as the source or drain are shown disposed on the main surface of a Pe^-type semiconductor substrate 9 on both sides of a gate electrode 12 that is formed on the main surface of the substrate 9 via a gate oxide film 11. A P^+-type region 30 having the same conductivity type as that of the substrate 9 but having a higher concentration is formed in advance by ion implantation or the like around the N^+-type region 14b on the right of the gate electrode 12 before the N^+-type region 14b is formed. The N^+-type region 14b is then formed inside this P^+-type region 30, thereby forming a double structure.

In the MOSFET structure described above, the left N^+-type region 14a, for example, is connected to the L level (the ground potential of the circuit) and the H level is applied to the right N^+-type region 14b (hereinafter, the H level will be referred to as the "drain voltage"). In other words, a case in which the N^+-type regions 14a and 14b are used as the source and drain regions, respectively, will be considered. The drain voltage expands the depletion layer at the boundary portion between the N^+-type region 14b and the P^+-type region 30. In this case, the depletion layer can be arranged to expand outside the P^+-type region 30 as represented by dotted line A in the drawing by suitably setting the drain voltage and the impurity concentration of the P^+-type region 30.

Under this state, when the H level is applied to the gate electrode 12 (hereinafter, this will be referred to as the "gate voltage"), a depletion layer is formed below the gate oxide film. At this time, the direction of the field inside the gate oxide film 11 is opposite on the drain side and the source side due to the influence of the drain voltage, so that an inversion layer CH is formed on the source side of the channel and extends towards the drain side. When the inversion layer reaches the depletion layer on the drain side, the electrons flowing through the inversion layer pass through the depletion layer and reach the drain region 14b, thus causing the drain current to flow.

On the other hand, in the MOSFET structure shown in Fig. 18, it will be assumed that the right N^+-type region 14b is connected to the ground potential and the drain voltage is applied to the left N^+-type region 14a, that is, the N^+-type regions 14a and 14b are used as the drain and source, respectively. Then, the expansion of the depletion layer becomes greater in the N^+-type region 14a as the drain than in Fig. 18, but the width of the depletion layer becomes smaller in the N^+-type region 14b as the source in which the inversion layer is formed, and becomes more inward than the boundary between the P^+-type region 30 and the substrate 9.

Therefore, it becomes difficult for the inversion layer to be formed in the channel portion which comes into contact with the gate oxide film 11 of the P^+-type region 30. In other words, the gate threshold voltage becomes higher when the left N^+-type region 14b is used as the source than when the N^+-type region 14b is used as the drain, as shown in Fig. 18.

As a result, in the MOSFET having the structure shown in Fig. 18, the threshold voltage comes to possess directivity. As a result of experiments, the inventors of the present invention confirmed that the threshold voltages vary depending upon the direction in the MOSFETs having the structure shown in Fig. 18.

If MOSFETs having four kinds of structures such as shown in Fig. 19 (A) through (D) are constituted as the memory cells using the MOSFET structure of Fig. 18 which can be constituted in such a manner that the threshold voltage can have the directivity as described above, two data can be stored in one memory cell.

The memory cell having the same structure as in the prior art cell such as shown in Fig. 19 (A) exhibits a low threshold voltage in both directions when both of the N^+-type regions 14a and 14b are used as the source or drain, and the data that becomes "0" and "0" of a binary signal can be stored.

If the right N^+-type region 14b has a double structure in which the P^+-type region 30 is formed around the N^+-type region 14b as shown in Fig. 19 (B), the threshold voltage is low when the N^+-type region 14b is used as the drain as described above, but becomes high when it is used as the source. Therefore, the memory cell shown in Fig. 19 (B) stores the data "0" and "1" in accordance with the read-out direction.

Similarly, if the left N^+-type region 14a has a double structure in which the P^+-type region 30 is formed around the N^+-type region, the threshold voltage is low when the N^+-type region 14a is used as the drain, and becomes high when it is used as the source. Therefore, the memory cell shown in Fig. 19 (C) stores the data "1" and "0" in accordance with the read-out direction.

Furthermore, if the P^+-type regions 30 are formed around the right and left N^+-type regions 14b and 14a, respectively, as shown in Fig. 19 (D), the threshold voltage is high even when either of these regions is used as the drain region, so that they can not turn on at the selection level of a suitable word line. Therefore, the data "1" and "1" for the two read-out direction is stored in the memory cell.

For the reasons described above, the memory capacity of the memory such as shown in Fig. 1 can be easily increased about twice without increasing the occupation area of the memory array in the memory by use of the MOSFETs having the directivity as described above.

Next, the memory cell array will be described in the following in connection with the specific construction thereof.

Fig. 20 is a top plan view showing an essential portion of the memory cell array for explaining the embodiment I of the present invention, and Fig. 21 is a sectional view taken along line XXI-XXI of Fig. 20. In Fig. 20 incidentally, the insulating films formed between the individual conductive layers are omitted so that the figure may be seen clearly.

In Figs. 20 and 21, like reference numerals are used to identify like portions as in Figs. 5 and 6, and the explanation of such portions will be omitted.

A P^+-type region 30 is formed on a P^--type semiconductor substrate 9 to write in the data 1. The area of the P^+-type region 30 is reduced as much as possible in order to prevent any adverse influences upon the threshold values of three MISFETs among four MISFETs sharing an N^+-type region 14. The P^+-type region 30 can be formed, for example, by implanting boron ions as a P-type impurity before or after the N^+-type region 14 is formed.

When the present invention is applied to the mask ROM, the data write-in operation becomes unnecessary, and hence the complicated circuit such as shown in Fig. 4 is not necessary. In other words, it is not necessary that the paired data line is selected by the decoder and the function of the selected data line is interchanged between the read-out operation and the write-in operation. This eliminates the necessity of the gate EX, and the function of selecting the paired data line becomes also unnecessary.

As a mask ROM circuit shown in Figs. 20 and 21, it is possible to obtain such a circuit by deleting the gate EX in Fig .4 and then applying directly the address signal A_0 from the address buffer circuit 5 to the inverter IV_1 and to the AND gates G_2, G_4 and G_6. Needless to say, the input buffer circuit 7 is not necessary.

It is also possible to use a circuit shown in Fig. 22. In Fig. 22, symbols Q_{13} through Q_{22} represent N-channel MOSFETs, symbol G_7 through G_{11} are AND gates, symbols G_{12} through G_{14} are OR gates, and a symbol IV_2 is an inverter. Symbols D_0 through D_4 represent the data lines, CD is a common data line and symbols C_0 through C_4 are output lines of the Y decoder 3.

Next, the read-out operation of the data written into the memory cell Q_{M1} in Fig. 22 will be described.

The Y decoder 3 sets only the output line C_0 to the H level and the other output lines $C_1 \sim C_4 \sim C_n$ to the L level on the basis of the address signals $A_1 \sim A_i$. As a result, since MOSFET Q_{13} becomes conductive, the data line D_0 is connected to the common data line CD, and since MOSFETs Q_{14} through Q_{17} become non-conductive, the data lines D_1 through D_4 ar cut off from the common data line CD. Among the gates G_{12} through G_{16}, it is only the gate G_{15} to which the H level is applied. Therefore, the gate G_{15} produces the H level, and the rest $G_{12} \sim G_{14}$ and G_{16} produce the L level. Since the gates G_7, $G_9 \sim G_{11}$ produce the L level irrespective of the level of the address signal A_0, MOSFETs Q_{18} and $Q_{20} \sim Q_{22}$ become non-conductive. The L level is applied as the address signal A_0 and is inverted by the inverter IV_2, and the H level is applied to one of the terminals of the gate G_8. In consequence, since the gate G_8 produces the H level, MOSFET Q_{19} becomes it euctive and the data line D_1 is set to the ground potential of the circuit.

The sense amplifier 8 detects whether or not the potential of the data line D_0, which is pre-charged to the H level, drops by setting the word line W_0 to the H level.

Next, in order to read out the other one bit data written into the memory cell Q_{M1}, only the output line C_1 is raised to the H level by new address signals A_1 through A_i with the other output lines being set to the L level. As a result, since MOSFET Q_{14} becomes conductive, the date line D_1 is connected to the common data line CD, and since MOSFETs Q_{13} and Q_{15} through Q_{17} become non-conductive, the data lines D_0, $D_2 \sim D_4$ are cut off from the common data line CD. It is only the gates G_{12} and G_{13} to which the H level is applied among the gates G_{12} through G_{16}. Therefore, these gates G_{12} and G_{13} produce the H level, while the rest produce the L level. Since the gates G_8, G_{10} and G_{11} produce the L level irrespective of the level of the address signal A_0, MOSFETs Q_{19}, Q_{21} and Q_{22} become non-conductive. As a result, the data lines D_3 and D_4 attain the floating state. Since the H level is applied as the address signal A_0, the H level is applied to the gate G_7 while the L level inverted by the inverter IV_2 is applied to the gate G9. In consequence, the gate G_7 produces the H level, thereby rendering MOSFET Q_{18} conductive and setting the data line D_0 to the ground potential of the circuit. On the other hand, since the gate G_9 produces the L level, MOSFET Q_{20} becomes non-conductive and the data line D_2 attains the floating state.

The sense amplifier 8 detects whether or not the potential of the data line D_1, which is pre-charged to the H level, drops by setting the word line W_0 to the H level.

Next, new address signals $A_0 \sim A_i$ are applied in order to read out the data written into the memory cell Q_{M2}. This address signal is to set the data line D_1 to the drain side and the data line D_2 to the source side. That is, the Y decoder 3 sets only the output line C_1 to the H level. The address signal A_0 is set to the L level. Therefore, the gate G_7, produces the L level, and the gate G_9 produces the H level, with the result that MOSFET Q_{18} becomes non-conductive, the data line D_0 attains the floating state, MOSFET Q_{20} becomes conductive and the data line D_2 is connected to the ground potential of the circuit. The sense amplifier 8 detects whether or not the potential of the data line D_1 drops.

As can be appreciated from the description given above, this is the system which determines the condition of the adjacent data lines by use of one of the address signals while one or two data lines adjacent to the data line connected to the memory cell are under the selectable state by use of the output of the Y decoder.

Moreover, as has been described hereinbefore, the following effects can be attained by the novel technical arrangement which is disclosed by the present application:

(1) Data of 2 (bits) can be held in a single MISFET by setting threshold voltage high or low at the side or sides of the source region and/or the drain region of the MISFET constructing the memory cell of the memory IC.

(2) Data for 2 (bits) can be held in a single MISFET by executing the writing of the data by alternately interchanging the data lines and the select lines. Read-out of the 2 (bits) can be effected by reading the first bit with the data and select lines in a first position and reading the second bit with the data and select lines interchanged.

(3) Since the data of 2 (bits) can be held in the single MISFET thanks to the foregoing effect (Q⅛(AND (2), the capacity of the memory IC can be increased to the remarkably high value.

(4) Data for 2 (bits) can be easily write in a single MISFET by implanting the hot carriers into the gate insulating film.

(5) By forming the thick insulating film 18 at the middle portion between the source region and the drain region, the hot carriers injected can be held stably in the gate insulating film at the side or sides of the source region and/or the drain region of the MISFET.

(6) Since, thanks to the foregoing effect (3), the hot carriers injected can be held stably in the gate insulating film at the side or sides of the source region and/or the drain region of the MISFET, it is possible to improve the reliability of the writing and reading operations of the data of the memory IC.

Although the invention conceived by us has been described specifically in connection with the embodiments thereof, the present invention should not be limited to the foregoing embodiments but can naturally be modified in various manners without departing from the gist thereof.

For example, although the invention has been described with particular reference to storing 2 bits per memory cell with the interchanging of the select line and data line to accomplish this, it should be noted that the arrangement of the present invention could be used to store 1 bit per memory cell with a fixed data line coupled to the drain and a fixed select line coupled to the source so that no line interchange occurs.

Also, although various voltage levels, layer thicknesses, etc. have been given, it should be noted that other values could be used while still falling within

the scope of the present invention. Besides the change of the threshold voltage, it is also possible to use a cell having a directivity in the mutual conductance g_m as the memory cell. Other means can be used as means for detecting the change of the potential of the data line besides the system using the sense amplifier described above.

CLAIMS

1. A semiconductor memory device comprising: a plurality of memory cells each comprised of an insulated field effect transistor having first and second semiconductor regions of a first conductivity type formed separately from one another in a substrate of a second conductivity type, an insulating film, a gate electrode on the insulating film, wherein each portion adjacent to said first region or said second region has one of the first threshold voltage and the second threshold voltage higher than said first threshold voltage in accordance with the data to be written in two bits into each of said memory cells.

2. A semiconductor memory device according to claim 1 wherein said second region having said second conductivity type is formed at said portion having said second threshold voltage.

3. A semiconductor memory device according to claim 1 wherein said second conductivity type is a p-type.

4. A semiconductor memory device according to claim 1 wherein carriers are injected to said insulating film of said portion having said second threshold voltage.

5. A semiconductor memory device according to claim 4, wherein said carriers are electrons.

6. A semiconductor memory device according to claim 5, wherein said memory cell has a read only memory function which can be erased by ultraviolet rays.

7. A semiconductor memory device according to claim 5, wherein said memory cell has a read only memory function which can be erased by an electrical signal.

8. A semiconductor memory device according to claim 4, wherein each of said insulated gate field effect transistors further comprises an additional insulating layer formed between said insulating film and said late electrode, said additional insulating layer being formed over a central portion of said insulating film over a portion of the substrate located between said portions adjacent to said first or second regions, and wherein said additional insulating layer has a greater thickness than said first insulating film.

9. A semiconductor memory device according to claim 4, wherein each insulated gate field effect transistor further comprises a floating gate electrode formed between said insulating film and said gate electrode, said floating gate electrode being separated from said gate electrode by a second insulating film.

10. A semiconductor memory device according to claim 1 which further comprises:
a first line coupled to said first region;
a second line coupled to said second region; and
means coupled to said insulated gate field effect transistors for supplying a high voltage to one of said first and second lines, a low voltage to the other of said first and second lines and a predetermined gate voltage to said gate electrode for a selected memory cell to read data out of said selected memory cell in accordance with whether the voltage level at said first or second line receiving the high voltage remains at the high voltage or drops when the predetermined gate voltage is applied to the gate in accordance with whether the written-in data has increased the threshold voltage of said insulated gate field effect transistor or not.

11. A semiconductor memory device according to claim 10 wherein the first bit of the selected memory cell is read out after said first and second lines are set to the high and low voltages, respectively, and wherein the second bit of the selected memory cell is read out after said first and second lines are set to the low and high voltages, respectively.

12. A semiconductor memory device according to claim 12 which further comprises:
a first line coupled to said first region;
a second line coupled to said second region; and
heans coupled to said insulated gate field effect transistors for supplying a first high voltage to one of said first and second lines, a low voltage to the other of said first and second lines and a predetermined gate voltage to said gate electrode for a selected memory cell to write data in to said selected memory cell, and
means coupled to said insulated gate field effect transistors for supplying a second high voltage lower than said first high voltage to one of said first and second lines, a low voltage to the other of said first and second lines and a high gate voltage to said gate electrode for a selected memory cell to read data out of said selected memory cell in accordance with whether the voltage level at said first or second line receiving the high voltage remains at the high voltage of drops when the predetermined gate voltage is applied to the gate in accordance with whether the written-in data has increased the threshold voltage of said insulated gate field effect transistor or not.

13. A semiconductor memory device according to claim 12 wherein the bit written into the selected memory cell under the state in which said first and second lines are set to said first high voltage and to said low voltage, respectively, is read out under the state in which said first and second lines are set to said low voltage and to said second high voltage, respectively.

14. A semiconductor memory device according to claim 12 wherein the first bit of the selected memory cell is written under the state in which said first and second lines are set to said first high voltage and to said low voltage, respectively; wherein the second bit of the selected memory cell is written under the stage in which said first and second lines are set to said low voltage and to said first high voltage, respectively; the first bit of the selected memory cell is read out after said first and second lines are set to said low voltage and to said second high voltage, respectively; and wherein the second bit of the selected memory cell is read out after said first and second lines are set to said second high voltage and to said low voltage, respectively.

15. A semiconductor memory device comprising:

a memory array having first data lines, second data lines and memory cells, each of said memory cells comprised of an insulated field effect transistor having first and second semiconductor regions formed separately from one another in a substrate, and capable of storing two-bits data;

said first and second data lines coupled to said first and second semiconductor regions;

a common data line to which said first and second data lines are to be coupled;

a ground potential line to which said first and second data lines are to be coupled; and

selecting means coupled to said first and second data lines;

said selecting means selecting one of said memory cells upon receiving address signals for said data lines, and coupling one of said first and second data lines of the selected memory cell to said common data line and the other of said first and second data lines to said ground potential line.

16. A semiconductor memory device according to claim 15 wherein said selecting means comprises first selecting means for selecting a plurality of said data lines coupled to or adjacent to said memory cells to be selected, among said first and second data lines, and second selecting means for coupling one of the two data lines coupled with said memory cell to be selected, among said selected data lines.

17. A semiconductor memory device according to claim 16 wherein said first selecting means selects one of the two data lines coupled to one memory cell, and said second selecting means couples the other of said data lines to said common data line.

18. A semiconductor memory device according to claim 16 wherein said second selecting means receives one bit of said address signal and said first selecting means receives the rest of said address signal.

19. A semiconductor memory device according to claim 18 wherein said one address signal is the most significant digit.

20. A semiconductor memory device according to claim 16 wherein each of said data lines has a first switch for the connection with said common data line and a second switch for the connection with said ground potential line.

21. A semiconductor memory device according to claim 16 wherein said first selecting means selects one of the two data lines connected to one memory cell and two data lines adjacent to said one data line, and said first selecting means couples said one data line to said common data line.

22. A semiconductor memory device according to claim 16 which further comprises an output circuit for reading out data of said memory cells, connected to said common data line.

23. A semiconductor memory device according to claim 22 wherein one of the two bits stored in one memory cell is read out under the state in which said first data line is coupled to said common data line and said second data line is coupled to said ground potential line when said first address signal is received, and the other of said two bits is read out under the state in which said first data line is coupled to said ground potential line and said second data line is coupled to said common data line when said second address signal is received.

24. A semiconductor memory device according to claim 17 which further comprises an input circuit for writing data into said memory cell coupled to said common data line, and an output circuit for reading out the data from said memory cell coupled to said common data line.

25. A semiconductor memory device according to claim 24 wherein one of the two bits stored in one memory cell is written under the state in which said first data line is coupled to said common data line and said second data line is coupled to said ground potential line when said first address signal is received, and the other of said two bits is written under the state in which said first data line is coupled to said ground potential line and said second data line is coupled to said common data line when said second address signal is received.

26. A semiconductor memory device according to claim 24 wherein said data written under the state in which said first data line is coupled to said common data line and said second data line is coupled to said ground potential line when said first address signal is received, is read out under the state in which said first data line is coupled to said ground potential line and said second data line is coupled to said common data line when said first address signal is received.

27. A semiconductor memory device according to claim 26 wherein said second selecting means receives one bit of said address signal, and said one-bit address signal at the time of read-out of the data is first converted to a signal which is the same as an inversion signal of said address signal at the time of write-in of the data, and is then supplied to said second selecting means.

28. A semiconductor memory device according to claim 25 wherein one of said bits is read out under the state in which said first data line is coupled to said ground potential line and said second data line is coupled to said common data line when said first address signal is received, and the other of said bits is read out under the state in which said first data line is coupled to said common data line and said second data line is coupled to said ground potential line when said second address signal is received.

Printed in the United Kingdom for Her Majesty's Stationery Office, 8818935, 10/85, 18996. Published at the Patent Office, 25 Southampton Buildings, London WC2A 1AY, from which copies may be obtained.